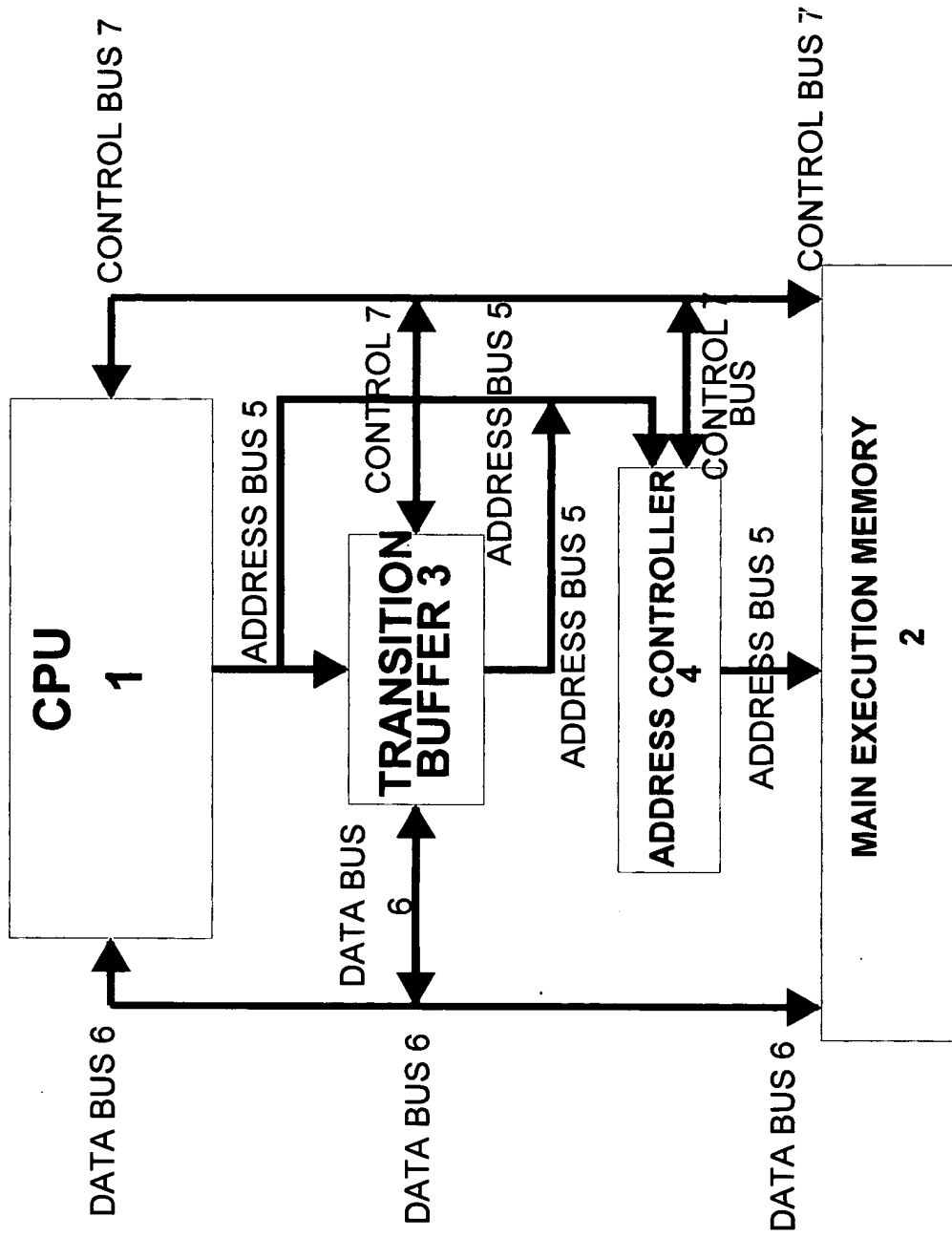
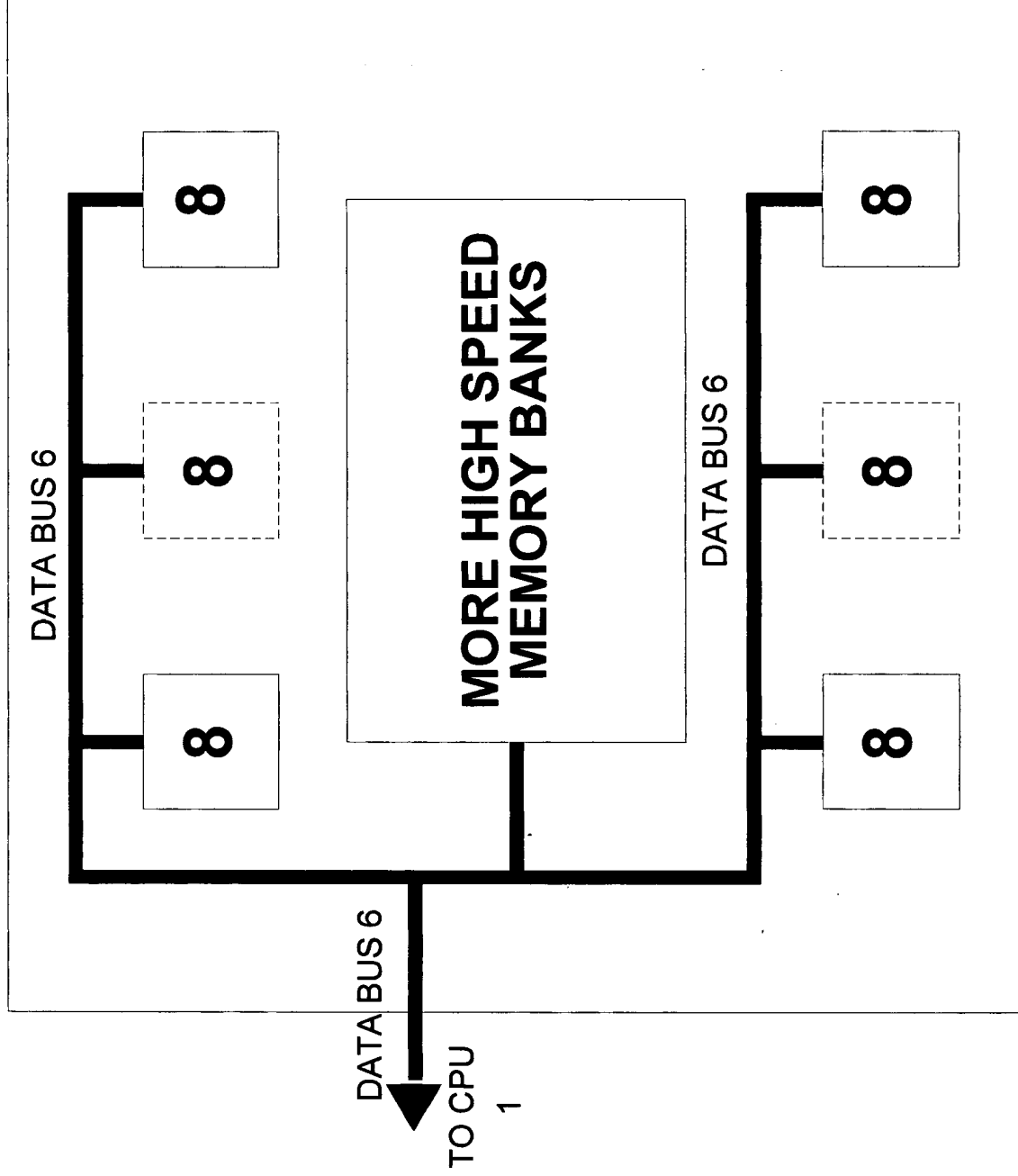


1 OF 12 SHEETS



ARCHITECTURAL REPRESENTATION OF CACHELESS COMPUTER SYSTEM

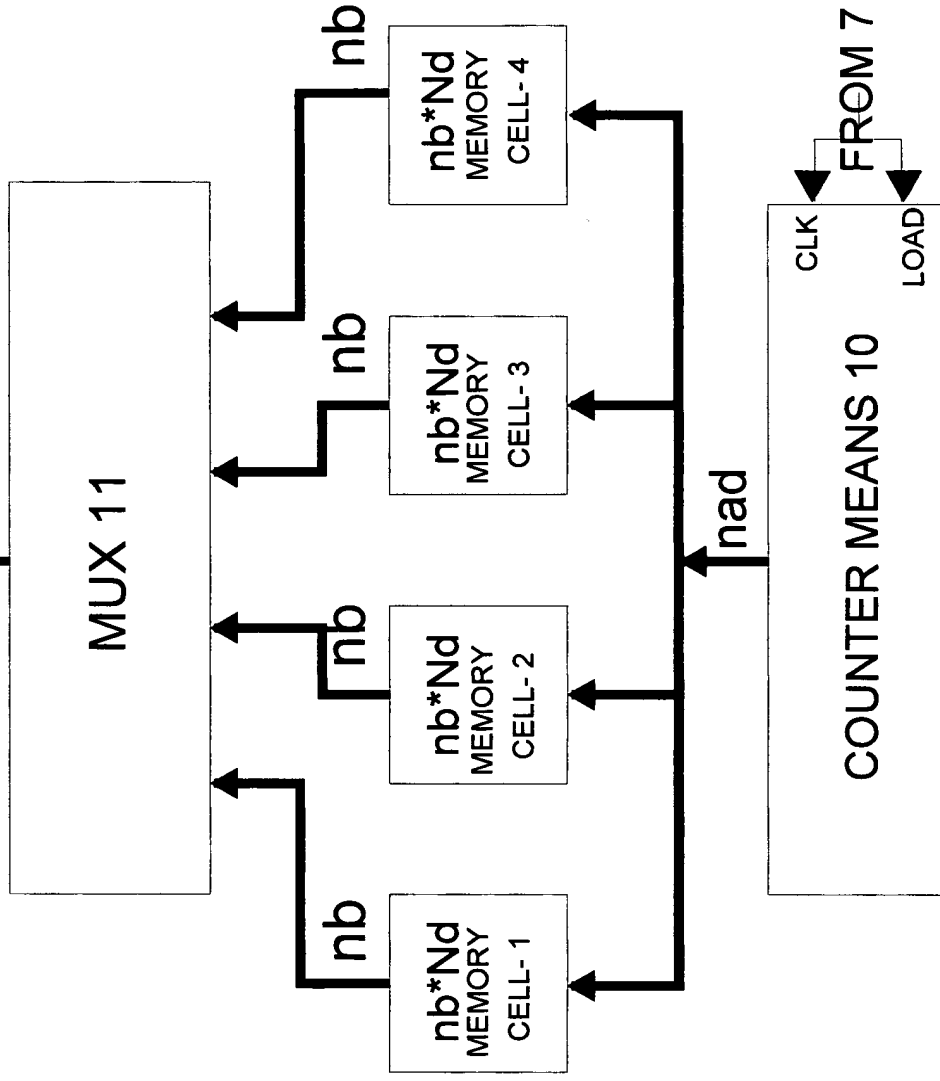
FIGURE - 1



MAIN EXECUTION MEMORY

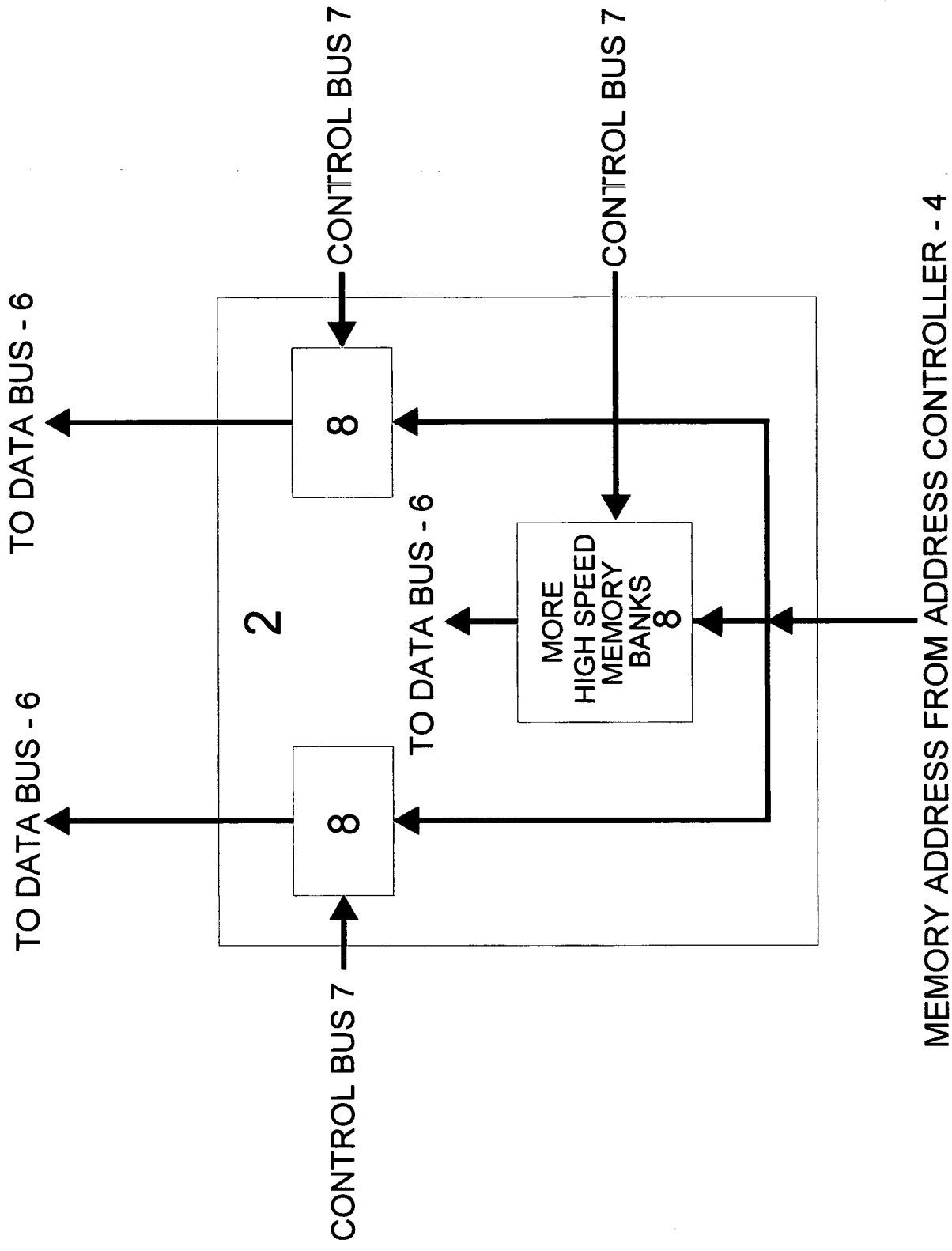
FIGURE - 2

TO DATA BUS - 6



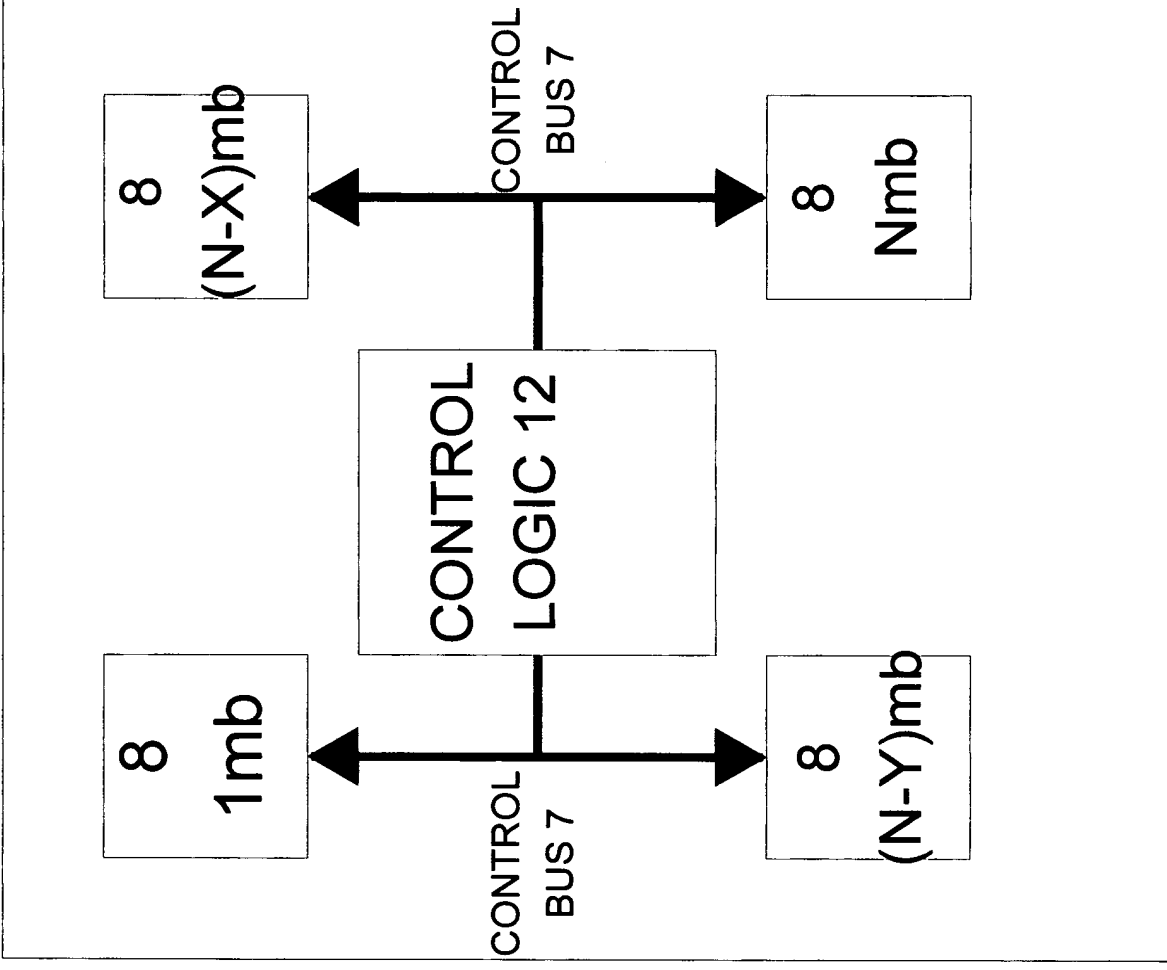
COUNT IN - FROM ADDRESS CONTROLLER - 4
HIGH SPEED MEMORY BANK

FIGURE 3



CONNECTION SCHEME FOR HIGH SPEED MEMORY BANKS

FIGURE 4



FLEXIBLE CONNECTION SCHEME FOR MAIN EXECUTION MEMORY

FIGURE 5

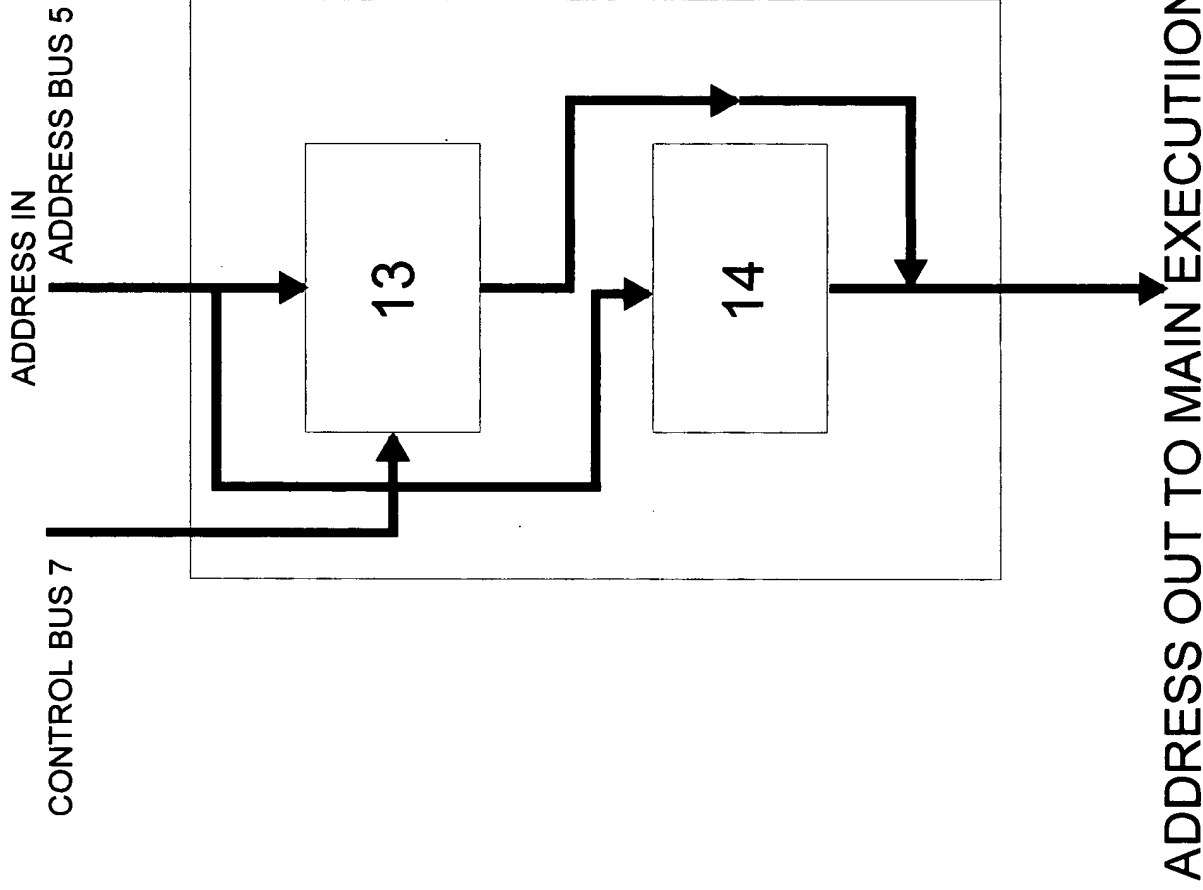
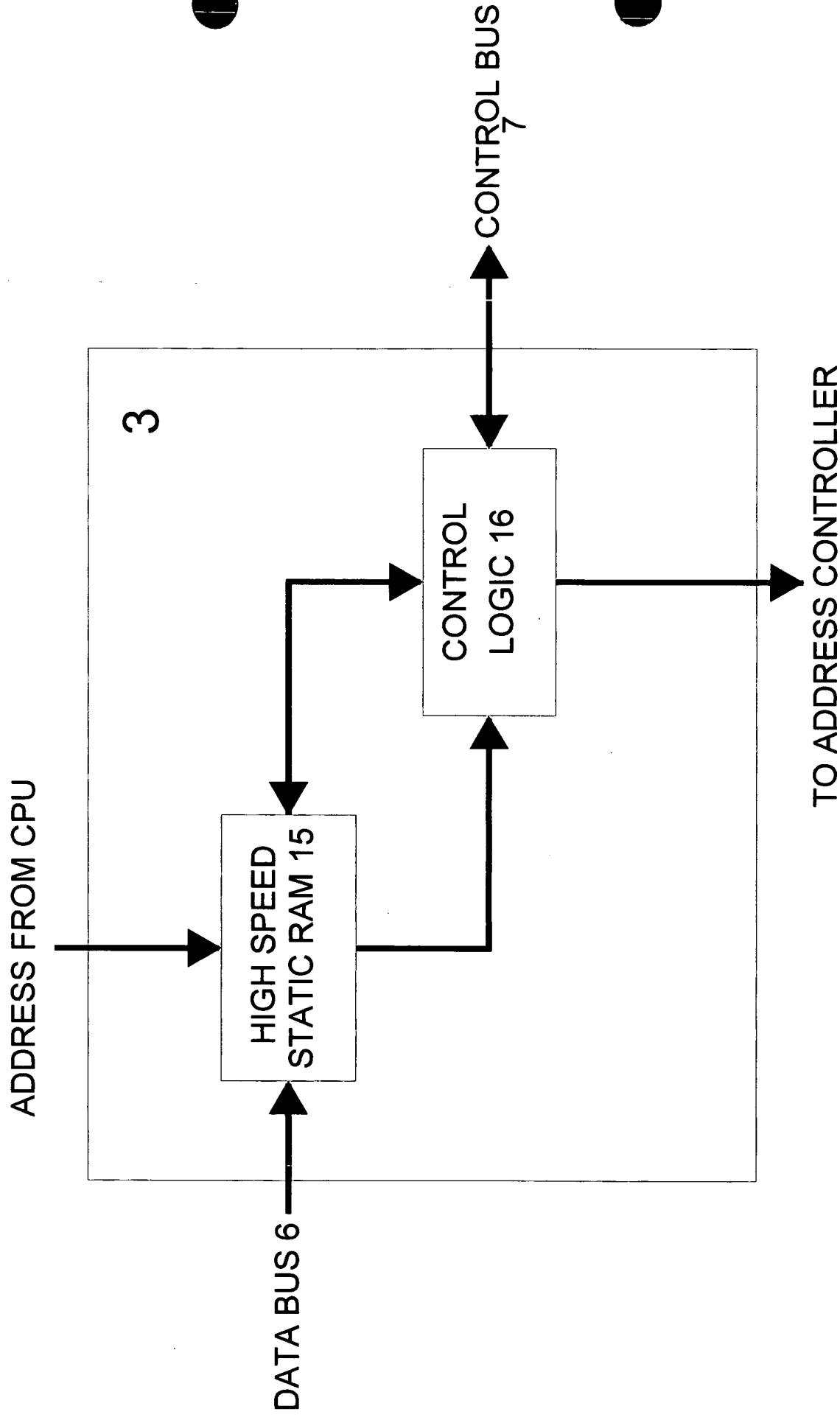
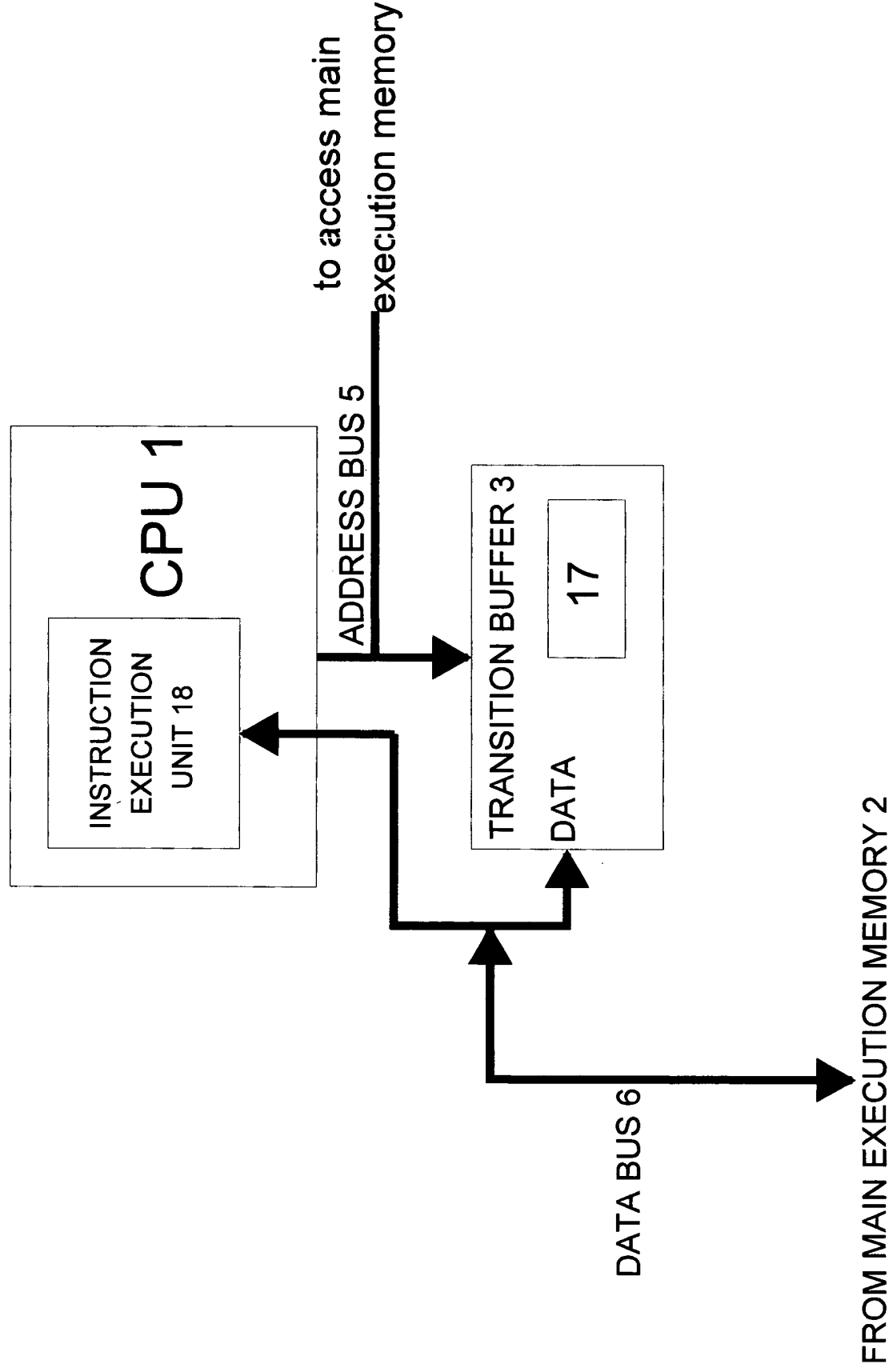


FIGURE 6

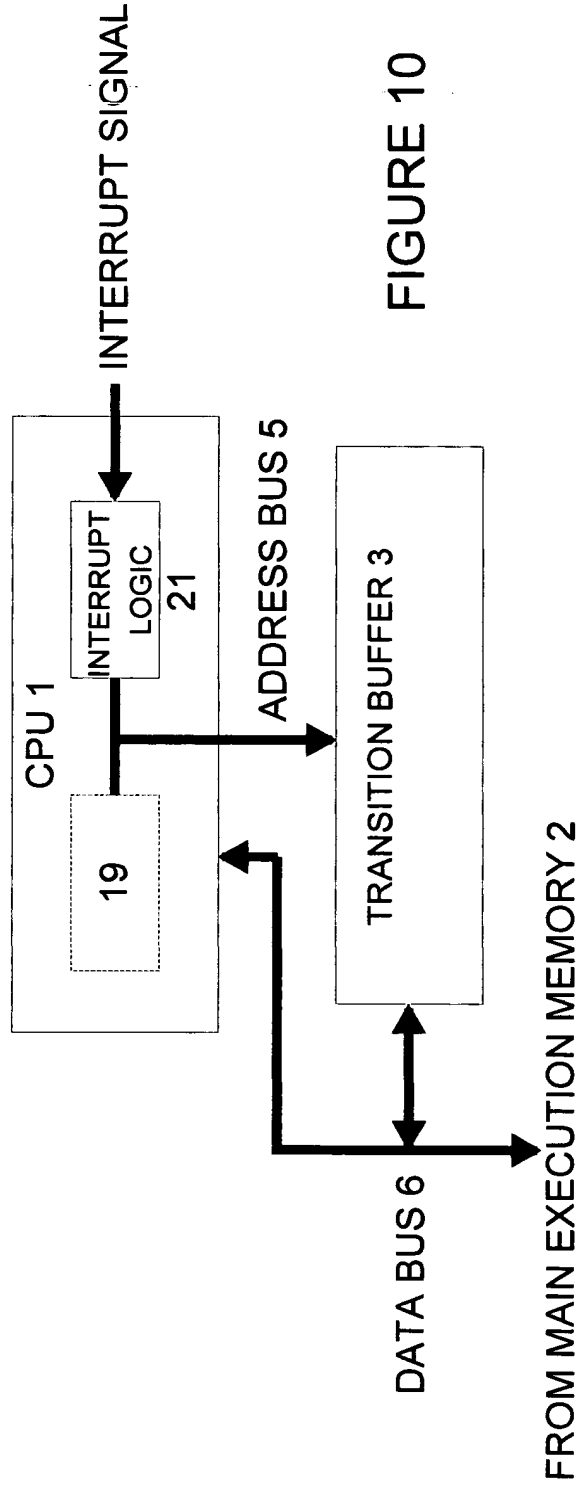
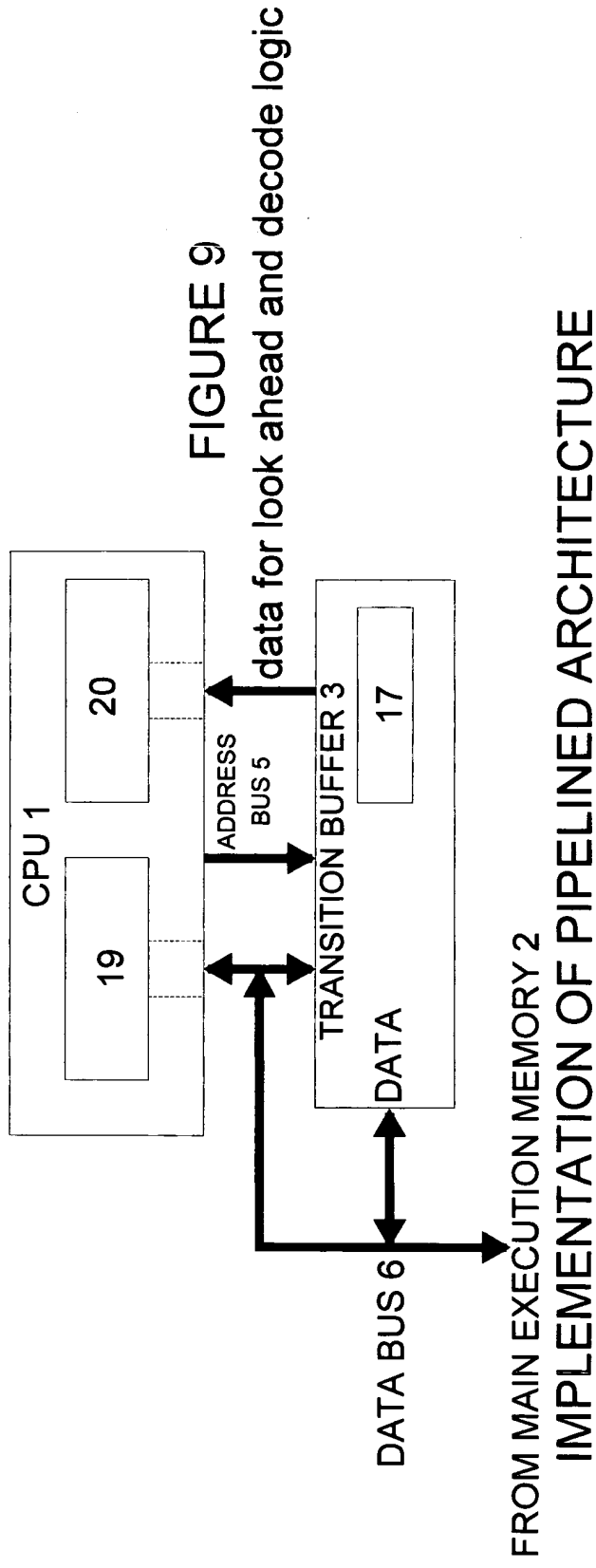


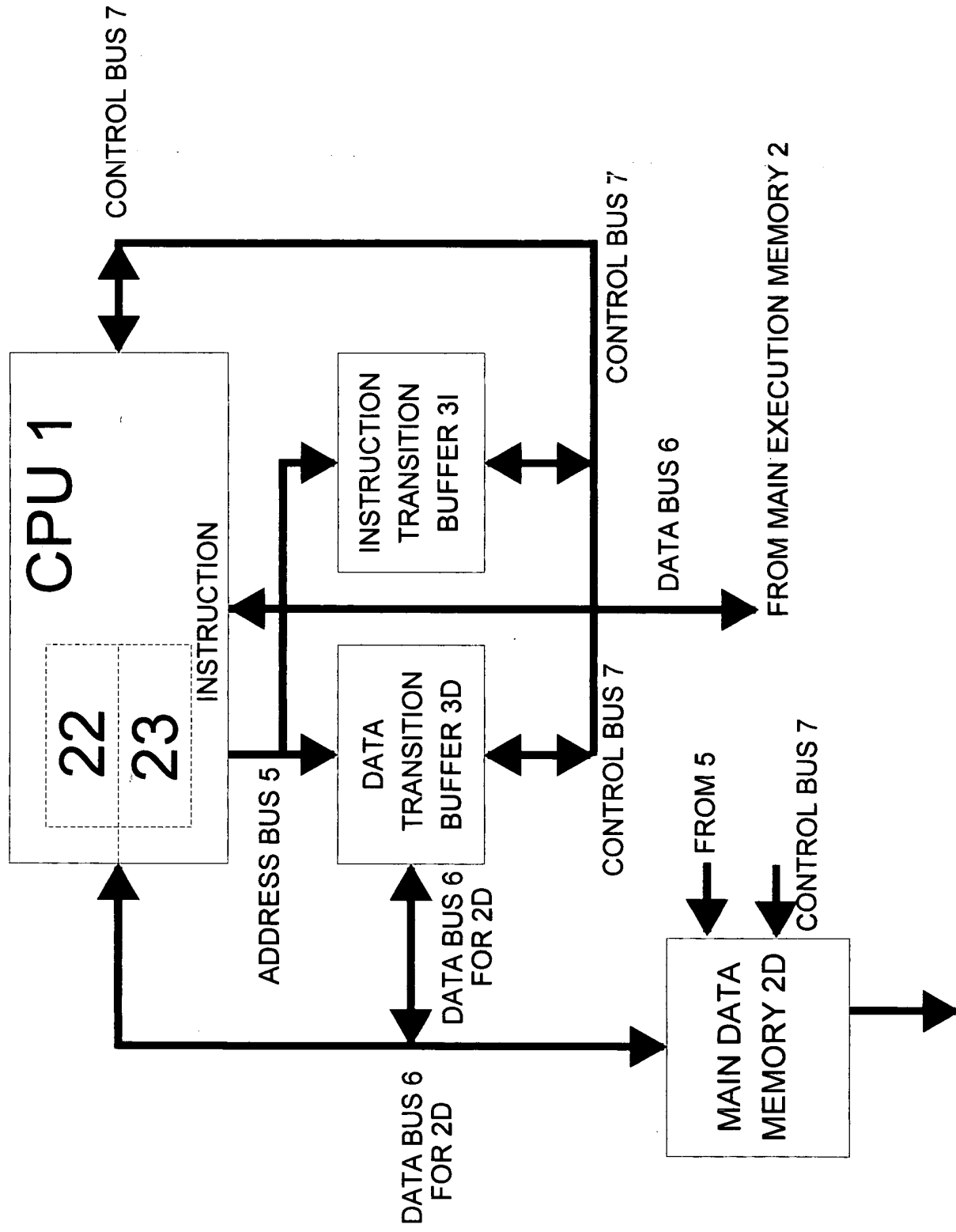
TRANSITION BUFFER
FIGURE 7



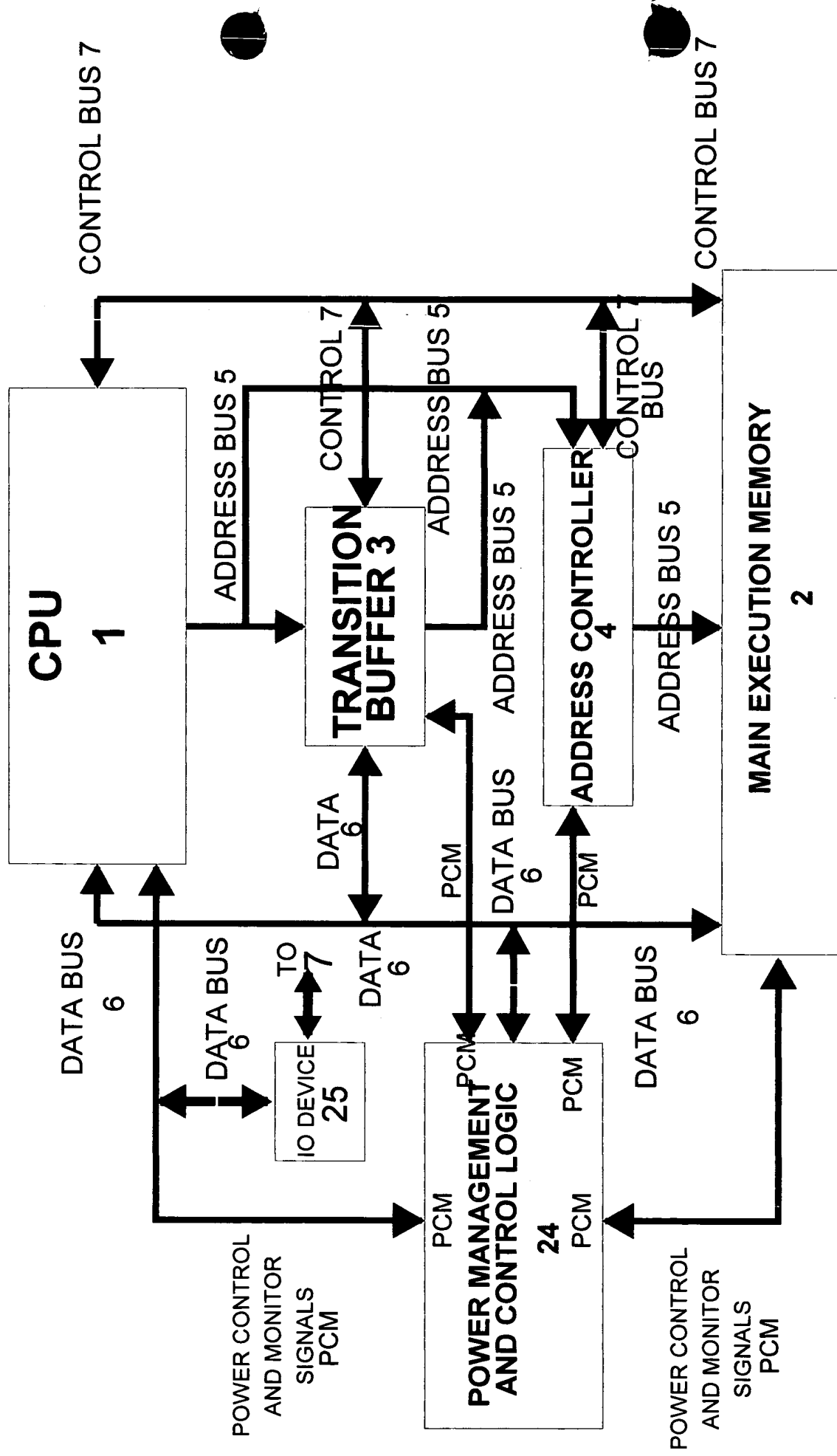
IMPLEMENTATION OF NON PIPELINED ARCHITECTURE

FIGURE 8

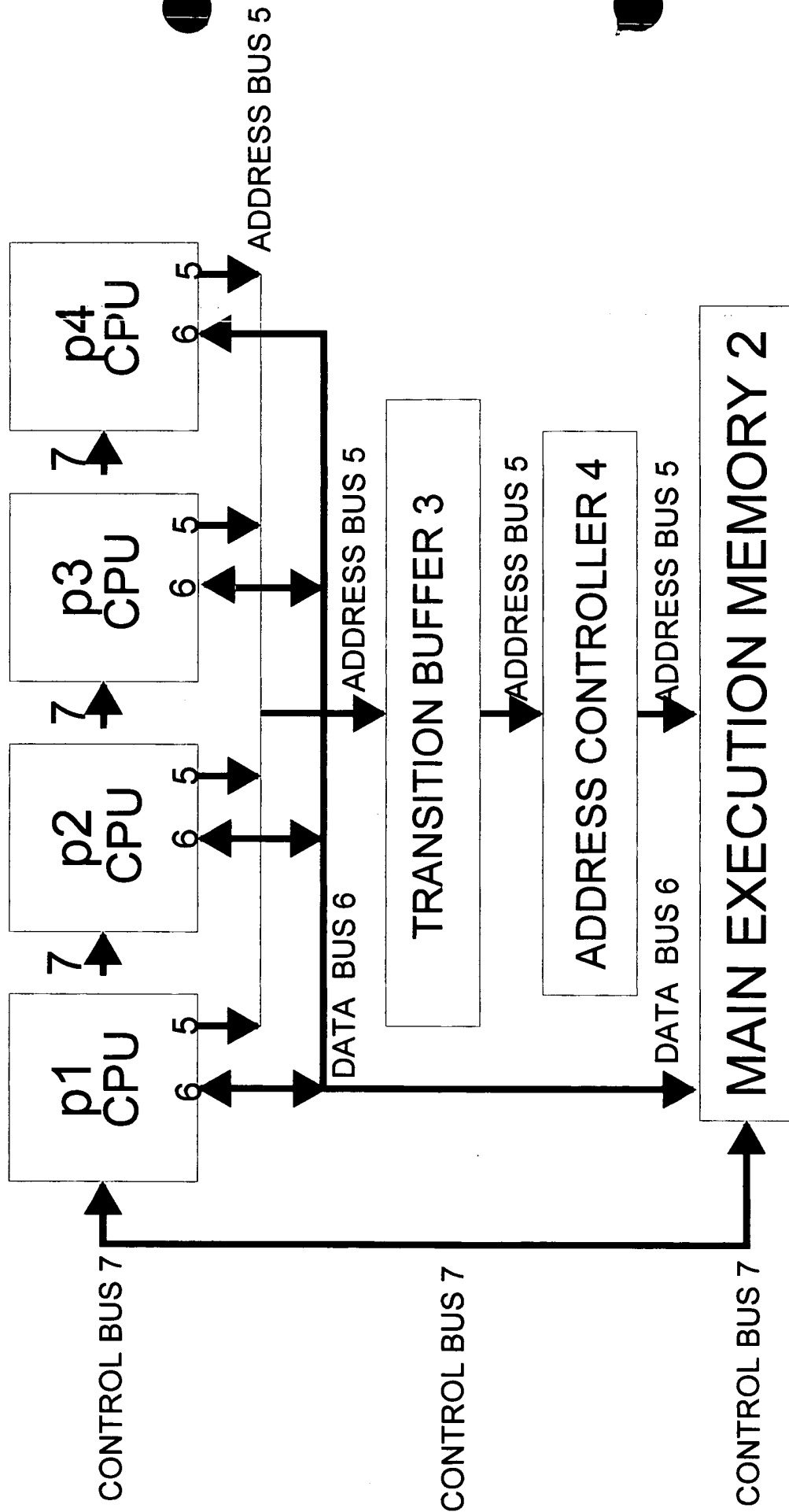




HARVARD ARCHITECTURE
FIGURE 11



POWER MANAGEMENT AND CONTROL LOGIC
FIGURE 12



PARALLEL OPERATION WITH MULTIPROCESSORS
FIGURE 13